Fabrication of conducting Si nanowire arrays

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The recent development of the superlattice nanowire pattern transfer technique allows for the fabrication of arrays of nanowires at a diameter, pitch, aspect ratio, and regularity beyond competing approaches. Here, we report the fabrication of conducting Si nanowire arrays with wire widths and pitches of 10–20 and 40–50 nm, respectively, and resistivity values comparable to the bulk through the selection of appropriate silicon-on-insulator substrates, careful reactive-ion etching, and spin-on glass doping. These results promise the realization of interesting nanoelectronic circuits and devices, including chemical and biological sensors, nanoscale mosaics for electronics, and ultradense field-effect transistor arrays. © *2004 American Institute of Physics*. [DOI: 10.1063/1.1801155]

As complementary metal-oxide semiconductor (CMOS) technology is scaled to the dimensions of a few nanometers, a key challenge is the manufacture of conducting silicon circuit elements at small dimensions and narrow pitch. Recent reports have partially addressed these challenges through, for example, the fabrication of the CMOS field-effect transistors (FETs) with gate lengths of 10–20 nm.[1] These studies constitute few device demonstrations of scaling feature size, and neglect considerations such as feature pitch, device-to-device reproducibility, and manufacturability—all of which are required for any robust application. For example, conducting 10–40 nm diameter silicon nanowires (NWs) have been demonstrated, as has the assembly of such NWs into small circuits.[2] However, issues such as quantitative doping control, the construction of large-scale conducting circuits, and circuit-to-circuit reproducibility have not been reported. In fact, the development of high-fidelity nanofabrication approaches constitutes a major scientific challenge to the field.

We describe the application of the superlattice nanowire pattern transfer[3] (SNAP) technique toward fabricating arrays of aligned, high aspect ratio silicon NWs with the goal of developing a reliable nanofabrication approach for creating ultrahigh density arrays with bulklike and controllable conductivity characteristics. Previous reports of the SNAP-generated arrays yielded the NWs down to 20-nm wide; only a fraction of those NWs conducted, and none exhibited bulklike conductivity characteristics.[3] We report here that Si NWs with widths of <30 nm are critically sensitive to the defects introduced by standard processing methods. For example, doping via ion implantation introduces defects within a silicon-on-insulator (SOI) film. Wires significantly smaller than 50 nm width (patterned on a 25 nm thick film) and longer than 10 μm will often contain at least one such defect, and the result is a poorly conducting wire. However, through a combination of careful substrate selection, spin-on glass doping, and low-energy, high-frequency fluorine-chemistry-based reactive ion etching (RIE), we demonstrate that Si NWs at diameters of 10 nm and larger, pitches of 40–50 nm, and lengths in excess of 1 mm can be fabricated with controllable, bulklike conductivity characteristics and useful field-effect transistor properties.

Samples were fabricated using a variation of the SNAP technique.[3] Briefly, the GaAs layers in a freshly cleaved $GaAs/Al_{0.5}Ga_{0.5}As$ superlattice are selectively wet etched to form a comb structure [Fig. 1(a)]. Platinum is then deposited along the ridges of the comb,[4] and the resulting Pt wires are gently pressed into a thin epoxy layer spun onto a SOI substrate. The superlattice templates are removed by wet-chemical etching, and an oxygen-plasma etch is utilized to

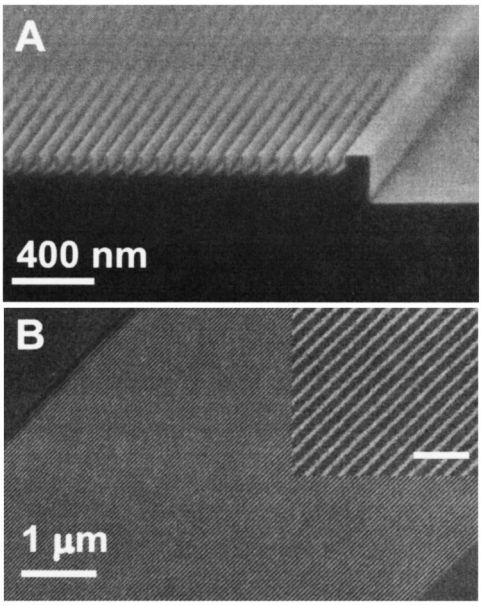

FIG. 1. Steps of the SNAP process utilized to fabricate the Si nanowire arrays are illustrated here. (a) The $GaAs/A1_{0.5}Ga_{0.5}As$ master, with the GaAs partially etched to produce the SNAP template. (b) 128 12 nm wide Si wires generated by using the Pt wires, formed onto and deposited from the template, as an etch mask. The inset reveals the structural fidelity of the nanowires at a higher resolution. The scale bar is 150 nm.

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remove the residual epoxy between the wires. The Pt wires serve as a shadow mask in the final dry etch used to transfer the NW pattern into the SOI substrate. The result is an array of Si NWs on an insulating oxide [Fig. 1(b)].

In order to maximize the NW conductivity, we investigated the relative importance of the defects native to our SOI substrates as compared to the defects introduced in the SNAP fabrication. A *p*-doped Si epilayer grown via molecular beam epitaxy (MBE) represented our "gold standard" for fabricating high-quality NWs; this substrate was used to test the RIE transfer of the NW pattern form Pt to Si. Those wires then served as a metric against which commercially available 4 and industry standard 8 in. SOI wafers were compared.[5] Additionally, the 4 in. SOI substrates were used to compared ion-implantation doping versus spin-on doping methods. These three factors—choice of starting material, etching chemistry, and doping method—are all essential for reliably obtaining conductive NWs below 50 nm in width.

The electrical resistivity of the Si NWs provides our figure of merit for NW quality. As a consequence, Si NW arrays were sectioned into multiple regions from 5 to 25 μm long,[6] and each section was contacted with four metal leads (Ti/Al/Pt 10 nm/150 nm/20 nm) then subsequently annealed to promote an ohmic contact (Ar;450°C;5 min). This allows for measurement of two sets of wires per region and for cross-conductance measurements between each set. The individual wires are 10–20 nm in width, depending on the process conditions, and two to four wires are addressed by each contact [Fig. 2(a), lower-right inset].

We employed a Unaxis SLR parallel-plate RIE system to maximize our control over the critical Si etch step. This tool employs a high-frequency power supply (40 MHz versus the more common 13.56 MHz), which generates a stable plasma at a dc bias as low as 10 V. An etch-gas mix of CF_4, H_2, and He provided protection for the Si sidewalls while attacking the exposed Si substrate.[7] This etch recipe achieved a pattern transfer with vertical Si sidewalls and no noticeable undercut, as observed with scanning electron microscopy (SEM).

Figure 2(a) (circle) shows a current-voltage (I–V) trace from a 7 μm long set of nanowires fabricated from the MBE substrate (30 nm B:Si on i-Si, $p=1\times10^{19}$ cm^{-3}); the linearity of the curve confirms the ohmic nature of the electrical contacts. A histogram representing several such measurements normalized by the bulk-scaled resistance, R_0, reveals the bulklike conductivity for these wires despite their narrow width of 10 nm [Fig. 2(b), top].[8] The good morphological properties of these NWs apparently correspond to good electronic properties, confirming that our etch recipe has prevented significant damage to the NWs.

In contrast, when the Si NWs were fabricated from the same substrate used in previous studies[3] (ion-implantation doped 4 in. SOI wafer; B:Si, 25 nm Si on 150 nm of oxide, $p=3\times10^{19}$ cm^{-3}), the R/R_0 histogram is centered near 10^4 (not shown), indicating that the electrical properties of those NWs are severely degraded. A probable defect source is lattice damage caused by the ion-implantation process. Using the ion-doped substrates, we find that we can use SNAP to fabricate highly conductive Si NWs down to 50 nm in width,

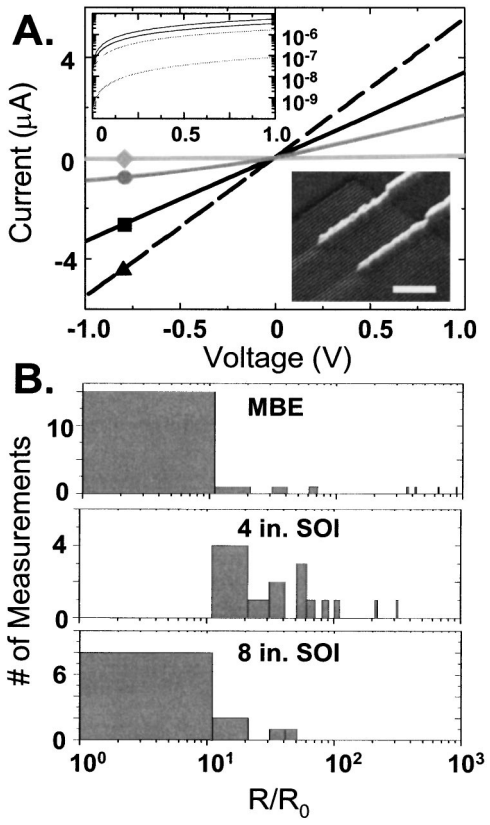

FIG. 2. (a) I–V measurements of four different nanowire samples: (square) 8 in. SOI, $p=5\times10^{19}$ cm^{-3} (10 nm×31 nm×3 μm), (triangle) 8 in. SOI, $n=1\times10^{20}$ cm^{-3} (10 nm×31 nm×3 μm) (circle) MBE, $p=1\times10^{19}$ cm^{-3} (10 nm×30 nm×7 μm), and (diamond) 4 in. SOI, $p=5\times10^{18}$ cm^{-3} (10 nm×25 nm×2.5 μm). (upper-left inset) The same data plotted on a semilog scale. (lower-right inset) An SEM of Ti/Al/Pt electrodes contacting three to four Si nanowires each, scale bar is 500 nm. (b) Statistical distribution of the nanowire resistance normalized by the bulk-scaled resistance (R_0) for wires fabricated from MBE substrates ($p=1\times10^{19}$ cm^{-3}), 4 in. SOI ($p=5\times10^{18}$ cm^{-3}), and 8 in. SOI ($p=5\times10^{19}$ cm^{-3}), respectively. The horizontal axis is log-scale and the bin size is 10.

but 10-25 nm wide wires are routinely poor conductors. We therefore explored spin-on doping as a batch-processing compatible doping alternative. The method utilizes high-temperature annealing to diffuse dopant atoms into the Si epilayer. A brief summary of our optimized process follows.

We used Emulsitone phosphorosilicafilm or Emulsitone borofilm[9] 100 (at dopant concentrations of 5×10^{20} cm^{-3}) diluted 1:10 in methanol as our *n*- and *p*-type dopant sources, respectively. The solutions were generously applied to a clean substrate surface; the wafer was spun at 4000 rpm for 30 s, and heated at 200°C to remove excess solvent. The substrate was then annealed under Ar, with the annealing conditions determined from a look-up table.[10] An *n*-type spin-on dopant matrix was removed with a buffered oxide etch (BOE) (6:1, NH_4F to HF), whereas a *p*-type matrix was removed using a hot 2:1, H_2SO_4:H_2O_2, followed by BOE.

To test the efficacy of this doping process, we fabricated the SNAP-patterned Si NWs using the spin-on doping method on the 4 in. SOI wafers (25 nm thick Si on 150 nm of oxide, sections 3-μm long, and $p=5\times10^{18}$ cm^{-3}). A slight nonlinearity in the current response at low voltages [Fig. 2(a), diamond] is recorded, although the measurements

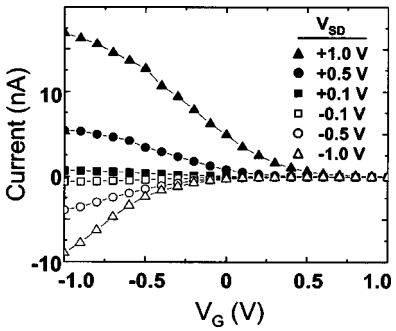

FIG. 3. Current response vs gate voltage, V_G, of a 7.5 μm long section of NWs fabricated from the 4 in. SOI wafer (cross section of 15×25 nm, $p=5\times10^{18}$ cm^{-3}) for a variety of different source-drain voltages, V_{SD}. The asymmetry in the source-drain bias is due to a difference in the Schottky-barrier height between the two contacts.

of the length-dependent resistance exhibit a linear scaling,[11] suggesting that the observed resistance values are dominated by the native wire conductivity. For these NWs, as for all the NWs fabricated from the SOI substrates, the resistance between the sets of NWs is found to be >1 T Ω. The resistance histograms of these NWs [Fig. 2(b), middle] reveal that, while their conductivity is worse than our gold standard by a factor of 10, it is significantly better than the ion-implantation-doped NWs. This result verifies ion-bombardment damage as the leading cause of suppressed conductivity in the latter NWs, and confirms the dominant physical mechanism underlying the suppressed conductivity observed in previous studies.[3]

A third potential source of defects is the method used to prepare the undoped SOI wafers: oxygen-ion bombardment and thermal annealing. This can result in conductivity-limiting defects in a fashion similar to that described for ion doping. Our SOI substrates have defect densities <0.1 cm^{-2} for the 8 in. (industry standard) wafer and 0.23 cm^{-2} for the 4 in. wafer. We also found a substantial leakage current through the insulating oxide of the 4 in. SOI wafer, but no such problems with the 8 in. wafer, implying that the 4 in. wafer was of lower quality. Figure 2(a) (square) and the bottom histogram in Fig. 2(b) show a representative current-voltage trace and normalized resistance values, respectively, for the SNAP Si NW arrays fabricated on 8 in. SOI wafers (30.8 nm thick Si on 145 nm of oxide, sections 3 μm long, and $p=5\times10^{19}$ cm^{-3}). The resistance histogram reveals the bulk scaling of the resistivity, validating our choices of substrate, doping technique, and etch recipe. We also prepared *n*-doped NWs on an 8 in. SOI substrate ($n=10^{20}$ cm^{-3}). A representative current-voltage scan of 3 μm long wires is shown in Fig. 2(a) (triangle, dashed line), confirming that our fabrication process is compatible with both the *p*- and *n*-type dopants. The normalized resistance data for *n*-type wires are consistent with that observed for *p*-type wires.

Finally, we assess the voltage response of these NWs by constructing a nano-FET structure. For this measurement, a 7 nm thick Al_2O_3 gate dielectric was deposited over a NW array fabricated from the 4-in. SOI wafer (7.5 μm long wires, $p=5\times10^{18}$ cm^{-3}), and a finger gate 250 nm wide was deposited across the NWs. As shown in Fig. 3, we were able to modulate the conductivity by 10^3 with a relatively modest gate voltage of $+/-1$ V. This voltage sensitivity is comparable to that of Si NWs grown using vapor-liquid-solid growth techniques[12] that have been shown to function as chemical and biological sensors,[13] suggesting that these NWs will also be suitable for that purpose. In addition, appropriate patterning of the gate oxide should enable the construction of a binary-tree multiplexer that can bridge length scales,[14] enabling us to address each wire within SNAP arrays with pitches as small as the current fabrication limit (16 nm) and beyond.

These results illustrate that ultrahigh density NW circuitry with reproducible, controllable, and bulklike electrical properties can be fabricated for Si NWs as small as 10 nm wide. Such high-quality circuits may be fabricated from commercially available and relatively inexpensive substrates using processing techniques derived from current practice. This result should provide a useful complement to existing techniques of nanowire synthesis that, while capable of producing high-quality wires in either single wire or batch fabrication,[15] pose significant challenges in terms of scalability, assembly, and manufacturability.

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[3] N. Melosh, A. Boukai, F. Diana, B. Gerardot, A. Badolato, P. M. Petroff, and J. R. Heath, Science **300**, 112 (2003).
[4] The Pt is deposited using an electron-beam evaporator and a self-aligned shadow mask technique. For the wires shown in Fig. 1, 8 nm of Pt was deposited at an evaporation angle of 15° above the plane of the sample.
[5] Ibis Technology Corporation, Danvers, MA.
[6] For the 4 in. SOI substrates, 75 nm of plasma enhanced chemical-vapor deposition grown oxide is deposited. This is followed by a selective etch to open windows above the nanowire sections.
[7] The full etch recipe is as follows: $CF_4/He/H_2$ at 20 sccm (denotes cubic centimeter per minute at STP) /30 sccm/2.5 sccm respectively, and an overall pressure of 5 mT. The rf power was 40 W and the etch time was determined using an end-point detector (interferometer). S. Wolf and R. N. Tauber, *Silicon processing for the VLSI era* (Lattice, Sunset Beach, California, 2000); *Handbook of advanced plasma processing techniques*, edited by R. J. Shul and S. J. Pearton (Springer, Berlin, 2000).
[8] This value is calculated using the dimensions of the nanowires as measured via the SEM and using the resistivity measured for the bulk substrate, assuming 3 NWs are contacted for each electrode. Fluctuations due to the varying numbers of wires contacted are not significant on the scale of the variation between the substrates.
[9] Emulsitone Company, Whippany, New Jersey.
[10] The look-up table was generated by measuring the four-point resistivity of a series of doped samples annealed at various temperatures and times. The temperatures ranged from 800 to 1000 °C and the times from 1 to 8 min.
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